MN80C48,MN80C49

CMOS 8-bit 1-chip Micromputers

■ Outline

The MN80C48 and MN80C49 are CMOS 8-bit 1-chip microcomputers which have ROM,RAM,I/O, timer and interrupt function integrated on 1 chip. They have different sizes of built-in ROMs and RAMs.

■ Features

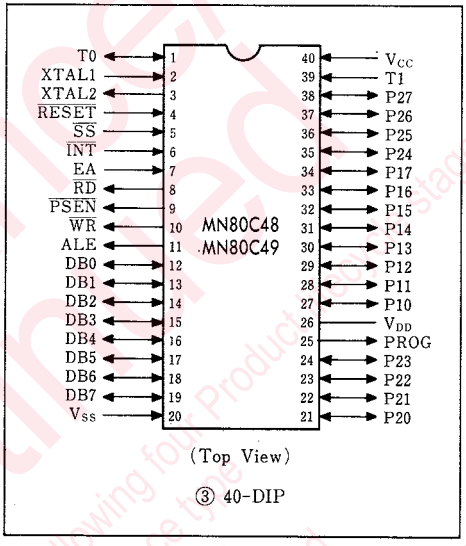
Hardware

- ROM capacity:2,048 x 8 bits(MN80C49)
  1,024 x 8 bits(MN80C48)
- RAM capacity:128 x 8 bits(MN80C49)
  64 x 8 bits(MN80C48)
- Interrupt:External interrupt pin × 1
- Timer/counter:8 bits × 1
- I/O pins:27 pins
  3 ports(8 bits for 1 port)
  3 test input pins,Single step function
- Execution speed(at 11 MHz):1.36μs
- ROM/RAM external extension:ROM 4 K, RAM 256 bytes
- Package:40-DIP(Compatible with Intel 80C48/80C49)

Software

- Instruction system with 96 kinds of instructions including addition, logical operation, decimal corrective operation and IDL instruction.
- 8 general purpose registers and 2 bank rigisters
- Low-power backup enabled by the Idle mode and Power-down mode

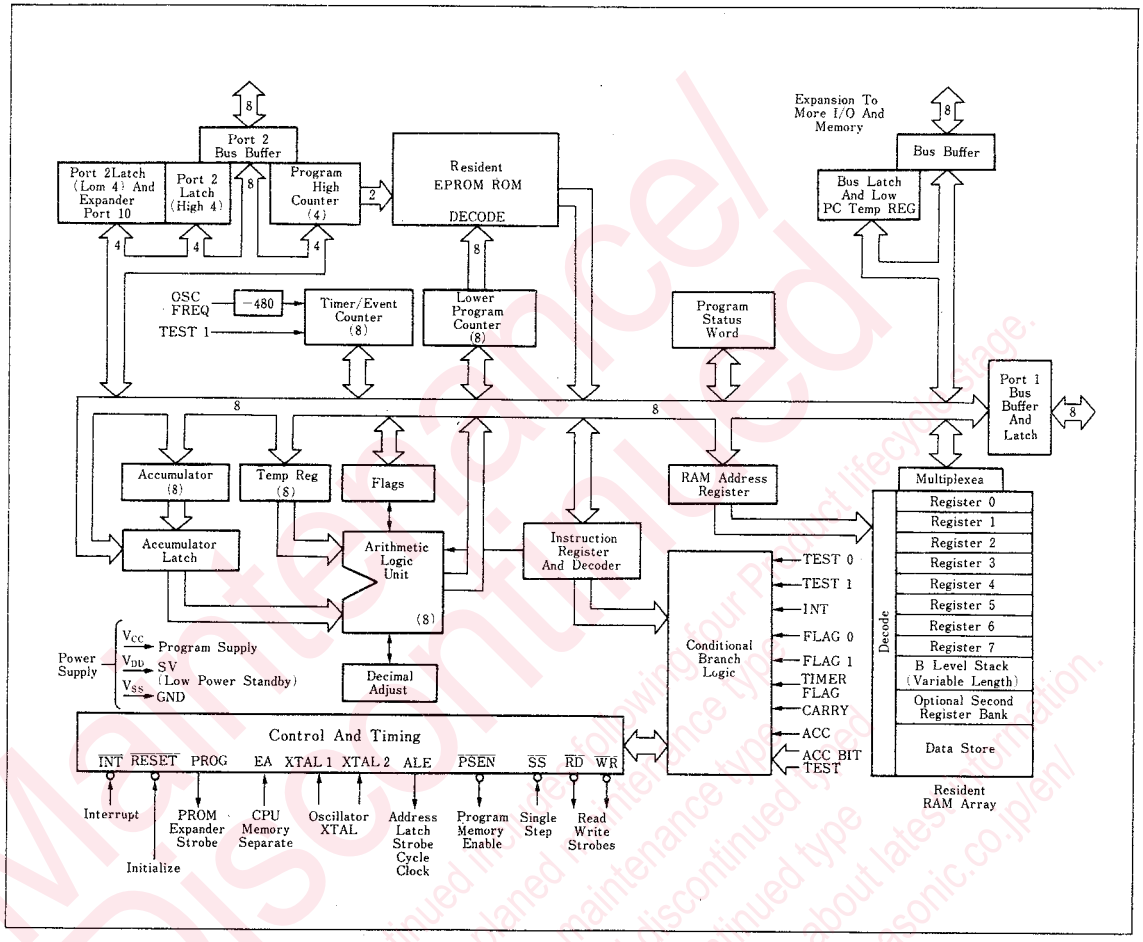
■ Pin Configuration



(Top View)

③ 40-DIP

■ Block Diagram



■ Absolute Maximum Ratings(V_{SS}=0 V, Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.5~+7.0	V
Input pin voltage	V_{IN}	−0.5~+7.0	V
Output pin voltage	V_{OUT}	−0.5~+7.0	V
Peak output current	$I_{OH(peak)}$	−0.5	mA
	$I_{OL(peak)}$	8	mA
Mean output current	$I_{OH(avg)}$	−0.25	mA
	$I_{OL(avg)}$	4	mA
Power disspation	P_D	1	W
Operating ambient temperture	T_{opr}	0~+70	°C
Storage temperture	T_{stg}	−65~+150	°C

■ Electrical Characteristics

● DC Characteristics($V_{CC}=V_{DD}=5V\pm20\%$, $V_{SS}=0V$, $Ta=0$ to $+70°C$)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply voltage	V_{CC}, V_{DD}		4.0	5.0	6.0	V
Supply current	I_{CC}	f=11MHz f=6MHz f=1MHz $I_{tot}=I_{CC}+I_{DD}$	— — —	— — —	15 8.5 4	mA mA mA
Idle mode	I_{Idle}	f=11MHz f=6MHz f=1MHz $I_{Idle}=I_{CC}+I_{DD}$	— — —	— — —	6 4 2.2	mA mA mA
Power-down mode	I_{pd}	$V_{DD}=2V$, $\overline{RESET}$=LOW	—	—	2	μA
Low-level input voltage Other than $\overline{RESET}$, XTAL1, XTAL2	V_{IL}		−0.5	—	$0.18V_{CC}$	V
Low-level input voltage RESET; XTAL1; XTAL2	V_{IL1}		−0.5	—	$0.13V_{CC}$	V
High-level input voltage Other than $\overline{RESET}$, XTAL1, XTAL2	V_{IH}		$0.2V_{CC}$ +1.2	—	V_{CC}	V
High-level input voltage $\overline{RESET}$; XTAL1; XTAL2	V_{IL1}		$0.7V_{CC}$	—	V_{CC}	V
Bus port Low-level output voltage	V_{OL}	$I_{OL}=2mA$	—	—	0.6	V
Low-level output voltage RD; WR; PSEN; ALE	V_{OL1}	$L_{OL}=1.8mA$	—	—	0.6	V
Low-level output voltage PROG	V_{OL2}	$I_{OL}=1mA$	—	—	0.6	V
(Other outputs than the above)	V_{OL3}	$I_{OL}=1.6mA$	—	—	0.6	V
Bus port high-level output voltage	V_{OH}	$-I_{OH}=400\mu A$	$0.75V_{CC}$	—	—	V
High-level output voltage $\overline{RD}$; $\overline{WR}$; PSEN; ALE	V_{OH1}	$-I_{OH}=100\mu A$	$0.75V_{CC}$	—	—	V
High-level output voltage (Other ports than the above)	V_{OH2}	$-I_{OH}=40\mu A$	2.4	—	—	V
$\overline{INT}$; T1; EA Input leakage current	$\pm I_{IL}$	Without internal pull-up $V_{SS}<V_I<V_{CC}$	—	—	10	μA
Bus input leakage current	$-I_{IL1}$	With internal pull-up $V_{SS}<V_I<V_{CC}$	—	—	500	μA
Input leakage current $\overline{RESET}$	$-I_{ILR}$	$V_{SS}<V_I<V_{IL1}$	10	—	300	μA
Output leakage current BUS, TO At high impedance	$\pm I_{OL}$	$V_{SS}<V_I<V_{CC}$	—	—	10	μA

● AC Characteristics

Item	Symbol	f(t)	11MHz			Unit
			min.	typ.	max.	
Clock width	t	$\frac{1}{X_{tal}}$	90.9		1000	ns
ALE pulse width	t_{LL}	3.5t−170	150		—	ns
Address setup time to ALE	t_{AL}	2t−110	70		—	ns
Address hold time from ALE	t_{LA}	t−40	50		—	ns
Control pulse width $\overline{RD}$, $\overline{WR}$	t_{CC1}	7.5t−200	480		—	ns
Control pulse width $\overline{PSEN}$	t_{CC2}	6t−200	350		—	ns
Data setup time to $\overline{WR}$	t_{DW}	6.5t−200	390		—	ns
Data hold time from $\overline{WR}$(Note 2)	t_{WD}	t−50	40		—	ns
Data hold time $\overline{RD}$, $\overline{PSEN}$	t_{DR}	1.5t−30	0		110	ns
$\overline{RD}$ to data input	t_{RD1}	6t−170	—		375	ns
$\overline{PSEN}$ to data input	t_{RD2}	4.5t−170	—		190	ns
Address setup time to $\overline{WR}$	t_{AW}	5t−150	300		—	ns
Address setup time to data input $\overline{RD}$	t_{AD1}	10.5t−250	—		730	ns
Address setup time to data input $\overline{PSEN}$	t_{AD2}	7.5t−220	—		460	ns
Address floating to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	2t−40	140		—	ns
Address floating to $\overline{RSEN}$	t_{AFC2}	0.5t−40	10		—	ns
ALE to control pulse $\overline{RD}$, $\overline{WR}$	t_{LAFC1}	3t−75	200		—	ns
AEL to control pulse $\overline{PSEN}$	t_{LAFC2}	1.5t−75	60		—	ns
$\overline{RD}$, $\overline{WR}$, $\overline{PROG}$ to ALE	t_{CA1}	t−40	25		—	ns
$\overline{PSEN}$ to ALE	t_{CA2}	4t−40	290		—	ns
Control setup to $\overline{PROG}$	t_{CP}	1.5t−80	50		—	ns
Port control hold to $\overline{PROG}$	t_{PC}	4t−260	100		—	ns
$\overline{PROG}$ hold time	t_{PR}	8.5t−120	—		650	ns
Data hold time from $\overline{PROG}$	t_{PF}	1.5t	0		140	ns
Output data setup time	t_{DP}	6t−290	250		—	ns
Output data hold time	t_{PD}	1.5t−90	40		—	ns
$\overline{PROG}$ pulse width	t_{PP}	10.5t−250	700		—	ns

● AC Characteristics(Continued)

Item	Symbol	f(t)	11MHz			Unit
			min.	typ.	max.	
Port 2 I/O data setup time to ALE	t_{PL}	4t-200	160		——	ns
Port 2 I/O data hold time to ALE	t_{LP}	1.5t-120	15		——	ns
Port output from ALE	t_{PV}	4.5t+100	——		510	ns
Cycle time	t_{CY}	15t	1.36		15	μs
T_0 repeat cycle	t_{OPRR}	3t	270		——	ns

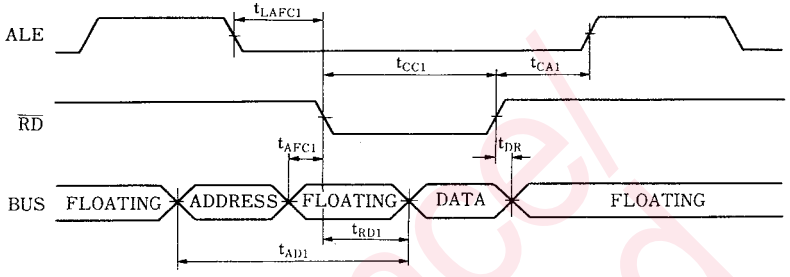
Note 1) Control output=C_L=80pF, Bus output=C_L=150pF
Note 2) Bus high impedance load=20pF

■ Pin Descriptions

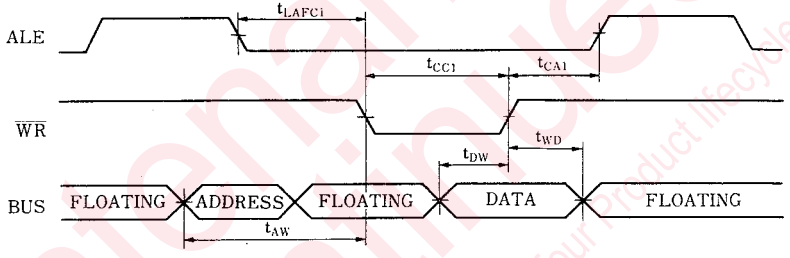
Pin No.	Symbol	I/O	Description
1	T0	I/O	Input pin for conditional branch instructions JT0, JNT0 or outputs oscillation ferquency clocks 1/3-divided by the ENTO-CLK instruction.
2 3	XTA1 XTA2	I O	Internal clock crystal connection pins. External clock input or input from XTAL1
4	$\overline{\text{RESET}}$	I	Resets the CPU through low-level input.
5	$\overline{\text{SS}}$	I	Single step operation. Low-level input causes the CPU to stop after terminating an instruction currently executed. At this time, ALE is held at the High level, and the next execution address is outputted to DB0-DB7 and P20-P23 in the extension mode.
6	$\overline{\text{INT}}$	I	External interrupt input pin. This is a level interrupt and must be held at the Low level until it is recognized as an interrupt. Also used as a JN1 instruction input pin to cancel the IDL mode.
7	EA	I	By impressing the High level(+5 V), access to the internal ROM is prohibited and the external ROM extension mode is set.
8	$\overline{\text{RD}}$	O	Outputed when reading the external data memory.(Active Low)
9	$\overline{\text{PSEN}}$	O	Outputted when fetching an instruction from exteranal ROM. (Active Low)
10	$\overline{\text{WR}}$	O	Outputed when writing in the external data memory.(Active Low)
11	ALE	O	Address latch strobe signal. Causes addressed data to be latched at a fall edge.
12~19	DB0~DB7	I/O	Serves as a bidirectional I/O port in the internal ROM mode, and as an address data bus in the external ROM extension mode.
20	V_{SS}	——	GND
21~24 35~38	P20~P23 P24~P27	I/O	8-bit dummy bidirectional ports. P20-P23 output upper 4 bits of an address in the external ROM extension mode.
25	PROG	O	Output strobe pin to the expander
26	V_{DD}	——	RAM power supply pin
27~34	P10~P17	I/O	8-bit dummy bidirectional ports
39	T1	I	Input pin for conditional branch instructions JT1 and JNT1. It also serves as an input pin for the STRTCNT instruction event counter.
40	V_{CC}	——	Normal operating power supply pin

■ Timing Diagrams

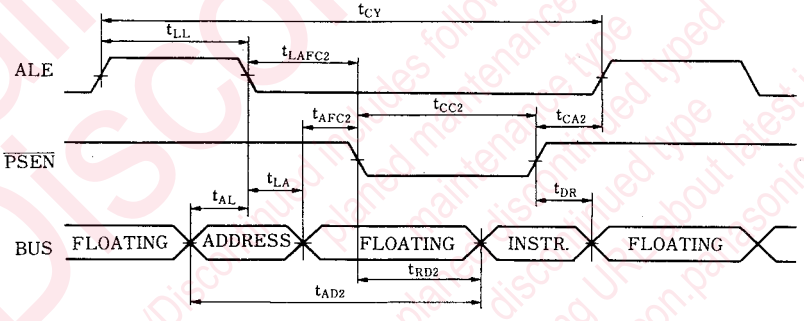
● External Data Memory Read Timing



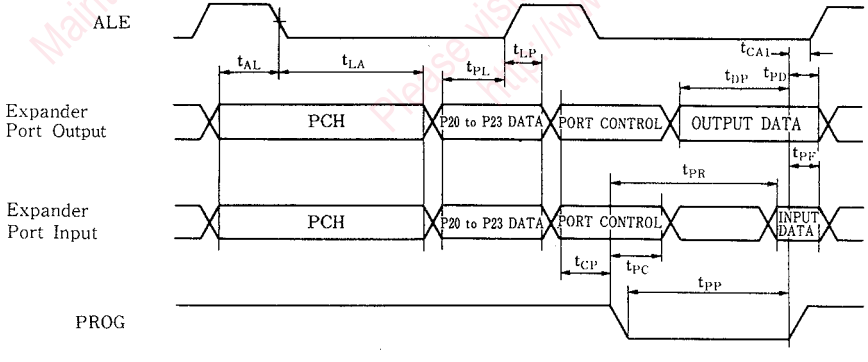
● External Data Memory Write Timing



● Instruction Fetch Timing from External Program Memory

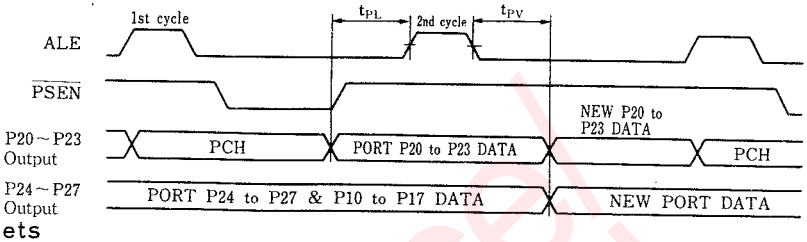


● Port 2 Timing



■ Timing Diagrams(Continued)

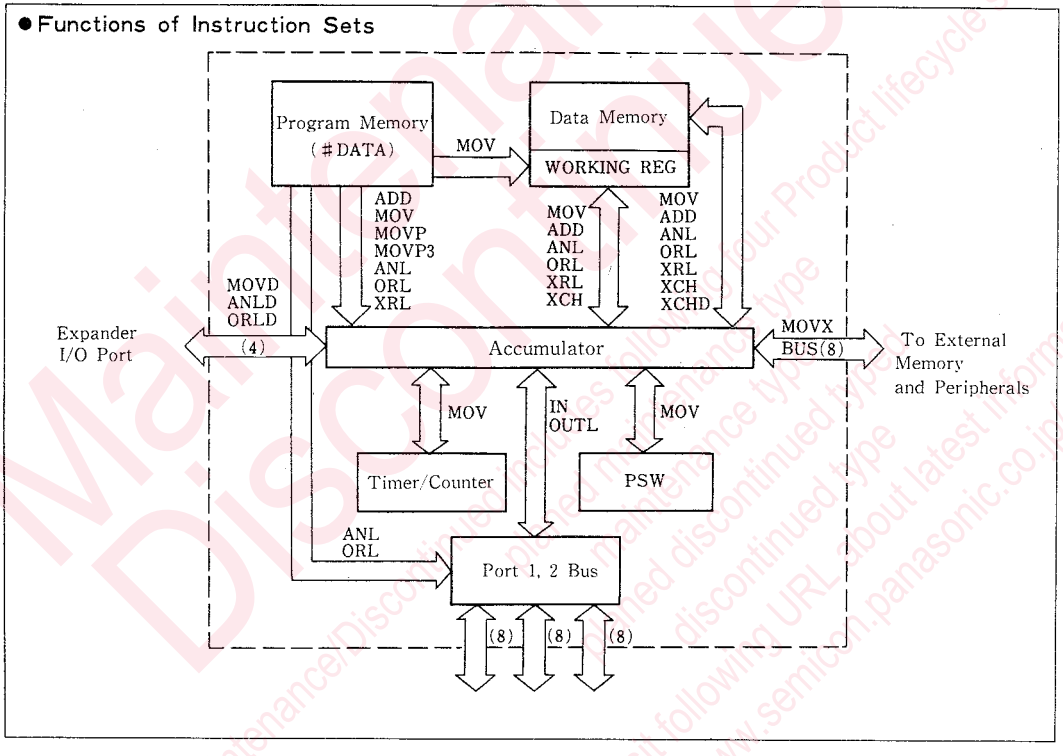
● I/O Port Timing



■ Instruction Sets

Instruction Sets for the MN80C48 and MN80C49 are grouped into ① Data transfer instructions, ② accumulator operational instructions, ③ register operational instructions, ④ flag operational instructions, ⑤ branch instructions, ⑥ subroutine instructions, ⑦ timer instructions, ⑧ control instructions, and ⑨ I/O instructions. The instructions consist of either 1 or 2 bytes; 70% or more of them are 1-byte instructions.

● Functions of Instruction Sets



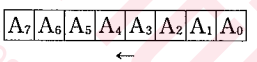
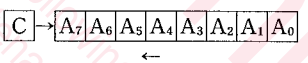
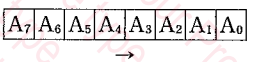
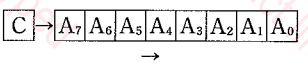
[Summary of Symbols and Abbreviations]

A	: Accumulator	PC	: Program counter
AC	: Auxiliary carry	Pp	: Port display(p=1, 2 or 4-7)
addr	: 12-bit program memory address or its part	PSW	: Program status word
Bb	: Bit display(b=0-7)	Rr	: Register display(r=0, 1 or 0-7)
BS	: Bank switch	SP	: Stack pointer
BUS	: BUS port	T	: Timer
C	: Carry	TF	: Timer flag
CLK	: Clock	T0, T1	: Test pin T0, test pin T1
CNT	: Counter	X	: Mnemonic for external RAM
D	: 4-bit mnemonic, that is, nibble	#	: Prefix symbol to indicate an immediate data
data	: 8-bit numeral or expression	@	: Prefix symbol to indicate an indirect address
DBF	: Memory bank flip-flop	$	: Current value of the program counter
F0, F1	: Flag F0, Flag F1	(X)	: Contents of X itself
I	: INterrupt	((X))	: Address contents address by X
P	: Mnemonic for operation within a "page"	←	: Substitution

■ Summary of Instruction Sets

Gr.	Mnemonic	D7	D6	D5	D4	D3	D2	D1	D0	Byte	Machine Cycle	Flags Affected C	Flags Affected AC	Description
Accumulator	ADD A, Rr	0	1	1	0	1	r_2	r_1	r_0	1	1	○	○	(A)←(A)+(Rr) r=0~7 Adds the contents of the register Rr to the accumulator.
	ADD A, @Rr	0	1	1	0	0	0	0	r_0	1	1	○	○	(A)←(A)+((Rr)) r=0~1 Adds the contents of the data RAM pointed by the register Rr to the accumulator.
	ADD A, #IMM	0	0	0	0	0	0	1	1	2	2	○	○	(A)←(A)+IMM Adds immediate data to the accumulator.
		IMM												
	ADDC A, Rr	0	1	1	1	1	r_2	r_1	r_0	1	1	○	○	(A)←(A)+(Rr)+(C) Rr=0~7 Adds the contents of the register Rr with carry, to the accumulator.
	ADDC A, @Rr	0	1	1	1	0	0	0	r_0	1	1	○	○	(A)←(A)+((Rr))+(C) Rr=0~1 Adds the contents of the data RAM pointed by the register Rr to the accumulator, with carry.
	ADDC A, #IMM	0	0	0	1	0	0	1	1	2	2	○	○	(A)←(A)+IMM+(C) Adds immediate data to the accumulator, with carry.
		IMM												
	ANL A, Rr	0	1	0	1	1	r_2	r_1	r_0	1	1	–	–	(A)←(A) (Rr) r=0~7 ANDs the accumlator and register Rr, and stores a result in the accumulator.
	ANL A, @Rr	0	1	0	1	0	0	0	r_0	1	1	–	–	(A)←(A) ((Rr)) r=0~1 ANDs the data RAM contents pointed by the accumulator Rr, and stores a result in the accumulator.
	ANL A, #IMM	0	1	0	1	0	0	1	1	2	2	–	–	(A)←(A) IMM ANDs the accumulator and immediate data, and stores a result in the accumulator.
		IMM												
	ORL A, Rr	0	1	0	0	1	r_2	r_1	r_0	1	1	–	–	(A)←(A) (Rr) r=0~7 ORs the accumulator and register Rr, and stores a result in the accumulator.
	ORL A, @Rr	0	1	0	0	0	0	0	r_0	1	1	–	–	(A)←(A) ((Rr)) r=0~1 ORs the data RAM contents pointed by the accumulator and Rr, and stores a result in the accumulator.
	ORL A, #IMM	0	1	0	0	0	0	1	1	2	2	–	–	(A)←(A) IMM ORs the accumulator and immediate data, and stores a result in the accumlator.
		IMM												
	XRL A, Rr	1	1	0	1	1	r_2	r_1	r_0	1	1	–	–	(A)←(A) (Rr) r=0~7 Exclusive ORs the accumulator and register Rr, and stores a result in the accumulator.
	XRL A, @Rr	1	1	0	1	0	0	0	r_0	1	1	–	–	(A)←(A) ((Rr)) r=0~1 Exclusive ORs the data RAM contents pointed by the accumulator and register Rr, and stores a result in the accumulator.

■ Summary of Instruction Sets(Continued)

Gr.	Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Byte	Machine Cycle	Flags Affected C	AC	Description
Accumulator	XRL A, #IMM	1	1	0	1	0	0	1	1	2	2	—	—	(A)←(A) IMM Exclusive ORs the accumulator and immediate data, and stores a result in the accumulator.
		IMM												
	INC A	0	0	0	1	0	1	1	1	1	1	—	—	(A)←(A)+1 Increments the accumulator.
	DEC A	0	0	0	0	0	1	1	1	1	1	—	—	(A)←(A)−1 Decrements the accumulator.
	CLR A	0	0	1	0	0	1	1	1	1	1	—	—	(A)←0 Clears the accumulator to 0.
	CPL A	0	0	1	1	0	1	1	1	1	1	—	—	(A)←(A) Inverts(assumes a complement of 1) the accumulator contents.
	DA A	0	1	0	1	0	1	1	1	1	1	○	—	Converts the accumulator contents into a 2−digit BCD code. If the upper 4 bits of the accumulator show a value larger than 9, or auxiliary carry is 1, 6 is added and 4 bits are similarly computed with carry taken into account.
	SWAP A	0	1	0	0	0	1	1	1	1	1	—	—	(A4~7)⇄(A3~0) Exchanges the upper 4−bit data of the accumulator for its lower 4−bit data.
	RL A	1	1	1	0	0	1	1	1	1	1	—	—	 Rotates the accumulator to the left by 1 bit. A7 is placed in A0.
	RLC A	1	1	1	1	0	1	1	1	1	1	○	—	 Rotates the accumulator to the left by 1 bit via carry. A7 is placed in C, and C in A0.
	RR A	0	1	1	1	0	1	1	1	1	1	—	—	 Rotates the accumulator to the rigth by 1 bit. A0 is placed in A7.
	RRC A	0	1	1	0	0	1	1	1	1	1	○	—	 Rotates the accumulator to the right by 1 bit via carry. C is placed in A7, and A0 in C.
Data Transfer	MOV A, Rr	1	1	1	1	1	r_2	r_1	r_0	1	1	—	—	(A)←(Rr) r=0~7 Transfers the contents of the register Rr to the accumulator.

■ Summary of Instruction Sets(Continued)

Gr.	Mnemonic	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Byte	Machine Cycle	Flags Affected C	Flags Affected AC	Description
Data Transfer	MOV A, @Rr	1	1	1	1	0	0	0	r_0	1	1	—	—	(A)←((Ri)) r=0~1 Transfers the data RAM contents pointed by the register Rr to the accumulator.
	MOV A, #IMM	0	0	1	0	0	0	1	1	2	2	—	—	(A)←IMM Transfers immediate data to the accumulator.
		IMM												
	MOV Rr, A	1	0	1	0	1	r_2	r_1	r_0	1	1	—	—	(Ri)←(A) r=0~7 Transfers the accumulator contents to the register Rr.
	MOV @Rr, A	1	0	1	0	0	0	0	r_0	1	1	—	—	((Rr))←(A) r=0~1 Transfers the accumulator contents to the data RAM pointed by the register Rr.
	MOV Rr, #IMM	1	0	1	1	1	r_2	r_1	r_0	2	2	—	—	(Rr)←IMM Transfers immediate data to the register Rr.
		IMM												
	MOV A, PSW	1	1	0	0	0	1	1	1	1	1	—	—	(A)←(PSW) Transfers the PSW contents to the accumulator.
	MOV PSW, A	1	1	0	1	0	1	1	1	1	1	—	—	(PSW)←(A) Transfers the accumulator contents to PSW.
	XCH A, Rr	0	0	1	0	1	r_2	r_1	r_0	1	1	—	—	(A) (Rr) r=0~7 Exchanges the accumulator contents for register Rr contents.
	XCH A, @Rr	0	0	1	0	0	0	0	r0	1	1	—	—	(A) (Rr) r=0~1 Exchanges the accumulator contents for the data RAM contents pointed by the register Rr.
	XCHD A, @Rr	0	0	1	1	0	0	0	r_0	1	1	—	—	(A0~3) ((Rr)0~3)r=0~1 Exchanges the lower 4−bit contents of the accumulator for those of the data RAM pointed by the register Rr.
	MOVP A, @A	1	0	1	0	0	0	1	1	1	2	—	—	(A)←((A)) Trasfers the contents of the program memory pointed by the accumulator to the accumulator.
	MOVP3 A, @A	1	1	1	0	0	0	1	1	1	2	—	—	(A)←((011)(A)) Trasfers the contents of the program memory on Page 3 pointed by the accumulator to the accumulater.
	MOVX A, @Rr	1	0	0	0	0	0	0	r_0	1	2	—	—	(A)←((Rr)) Trasfers the external data memory to the accumulator.
	MOVX @RrA	1	0	0	1	0	0	0	r_0	1	2	—	—	((Rr))←(A) Trasfers the accumulator contents to the external memory.
I/O	IN A, Pn	0	0	0	0	1	0	P_1	P_0	1	2	—	—	(A)←(Pn) n=1.2 Inputs data from the Port Pn to the accumulator.
	OUTL Pn, A	0	0	1	1	1	0	P_1	P_0	1	2	—	—	(Pn)←(A) n=1.2 Outputs accumulator data to the Port Pn to latch it.
	ANL Pn, #IMM	1	0	0	1	1	0	P_1	P_0	2	2	—	—	(Pn)←(Pn) IMM n=1, 2 ANDs port data and immediate data, and outputs it to the Port Pn.
		IMM												
	ORL Pn, #IMM	1	0	0	0	1	0	P_1	P_0	2	2	—	—	(Pn)←(Pn) IMM n=1, 2 ORs port data and immediate data, and outputs to the Port Pn.
		IMM												

Gr.	Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Byte	Machine Cycle	Flags Affected C	AC	Description
I/O	INS A,BUS	0	0	0	0	1	0	0	0	1	2	—	—	(A)←(BUS) When the RD signal is at the Low level, BUS port data is inputted to the accumulator.
	OUTL BUS, A	0	0	0	0	0	0	1	0	1	2	—	—	(BUS)←(A) The accumulator contents are latched and outputted to the BUS port.
	ANL BUS, #IMM	1	0	0	1	1	0	0	0	2	2	—	—	(BUS)←(BUS) IMM ANDs the BUS port and immediate data, and outputs to the BUS port.
		IMM												
	ORL BUS, #IMM	1	0	0	0	1	0	0	0	2	2	—	—	(BUS)←(BUS) IMM ORs the BUS port and immediate data, and outputs to the BUS ports.
		IMM												
	MOVD A, Px,	0	0	0	0	1	1	P_1	P_0	1	2	—	—	(A)0~3←(Px)(A)4~7←0 X=4~7 Inputs the data of the extension ports 4−7 with the 8243 used to the accumulators A0−A3. A4−A7 are reset.
	MOVD Px, A	0	0	1	1	1	1	P_1	$P_\pm$	1	2	—	—	(Px)←(A)0~3 X=4~7 Outputs the contents of the accumulators A0−A3 to the extension ports 4−7 with the 8243 used. A4−A7 are not changed.
	ANLD Px, A	1	0	0	1	1	1	P_1	P_0	1	2	—	—	(Px)←(Px) (A)0~3 X=4~7 ANDs the extension ports 4−7 and accumulators A0−A3, and outputs its result to the extension port Px.
	ORLD Px, A	1	0	0	0	1	1	P_1	P_0	1	2	—	—	(Px)←(Px) (A)0~3 X=4~7 ORs the extension ports 4−7 and accumulators A0−A3, and outputs its result to the extension port Px.
Register	INC Rr	0	0	0	1	1	r_2	r_1	r_0	1	1	—	—	(Rr)←(Rr)+1 r=0~7 Increments the register Rr contents.
	INC @Rr	0	0	0	1	0	0	0	r_0	1	1	—	—	((Rr))←((Rr))+1 r=0~1 Increments the RAM contents pointed by the register Rr.
	DEC Rr	1	1	0	0	1	r_2	r_1	r_0	1	1	—	—	(Rr)←(Rr)−1 r=0~7 Decrements the register Rr contents.
Branch	JMP addr	a_{10}	a_9	a_8	0	0	1	0	0	2	2	—	—	(Pc)0~10←a0~a10, (Pc)11←MBF A memory bank flag is set for(Pc) 11 which jumps to a program area within 2K.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JMPP @A	1	0	1	1	0	0	1	1	1	2	—	—	(Pc)0~7←((A)) The program memory contents pointed by the accumulator are set to(Pc)0−7.
	DJNZ Rr, addr	1	1	1	0	1	r_2	r_1	r_0	2	2	—	—	(Rr)←(Rr)−1 (Pc)0~7←a0~a7 Rr=0~7 Decrements the register Rr contents by 1, and branches to A0−A7 if its result is not zero.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JC addr	1	1	1	1	0	1	1	0	2	2	—	—	(Pc)0~7←a0~a7 at C=1 (Pc)0~7←(Pc)0~7+2 at C=0 Jumps to a specified address when carry is 1.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JNC addr	1	1	1	0	0	1	1	0	2	2	—	—	(Pc)0~7←a0~a7 at C=0 (Pc)0~7←(Pc)0~7+2 at C=1 Jumps to a specified address when carry is 0.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					

Gr.	Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Byte	Machine Cycle	Flags Affected C	AC	Description
Branch	JZ addr	1	1	0	0	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at A=0 (Pc)0～7←(Pc)0～7+2 at A=0 Jumps to a specified address when an accumulator value is 0.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JNZ addr	1	0	0	1	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at A≠0 (Pc)0～7←(Pc)0～7+2 at a=0 Jumps to a specified address when an accumulator value is not 0.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JT0 addr	0	0	1	1	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at T0=1 (Pc)0～7←(Pc)0～7+2 at T0=0 Jumps to aspecified address when the test pin T0 is "1"(high).
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JNT0 addr	0	0	1	0	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at T0=0 (Pc)0～7←(Pc)0～7+2 at T0=1 Jumps to a specified address when the test pin T0 is "0"(Low).
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JT1 addr	0	1	0	1	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at T1=1 (Pc)0～7←(Pc)0～7+2 at T1=0 Jumps to a specified address when the test pin T1 is "1"(High).
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JNT1 addr	0	1	0	0	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at T1=0 (Pc)0～7←(Pc)0～7+2 at T1=1 Jumps to a specified address when the test pin T1 is "0"(Low).
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JF0 addr	1	0	1	1	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at F0=1 (Pc)0～7←(Pc)0～7+2 at F0=0 Jumps to a specified address when the flag F0 is "1".
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JF1 addr	0	1	1	1	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at F1=1 (Pc)0～7←(Pc)0～7+2 at F1=0 Jumps to a specified address when the flag F1 is "1".
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JTF addr	0	0	0	1	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at TF=1 (Pc)0～7←(Pc)0～7+2 at TF=0 Jumps to a specified address when the timer flag is "1".
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JNI addr	1	0	0	0	0	1	1	0	2	2	—	—	(Pc)0～7←a0～a7 at I=1 (Pc)0～7←(Pc)0～7+2 at I=0 Jumps to a specified address if an external interrupt pin is at Low.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
	JBb addr	b_2	b_1	b_0	1	0	0	1	0	2	2	—	—	(Pc)0～7←a0～a7 at (bn)=1 (Pc)0～7←(Pc)0～7+2 at (bn)=0 Tests the accumulator bit specified with bn, and jumps to a specified address if "1".
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
Subroutine	CALL addr	a_{10}	a_9	a_8	1	0	1	0	0	2	2	—	—	((SP))←(Pc), (PSW)4～7 (SP)←(SP)+1 (Pc)8～10←A8～A10 (Pc)0～7←A0～A7 The program counter and PSW bits 4－7 are stored in the stack and the stack pointer is decremented by 1. Then, jumps to specified program bank and address.
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0					
		1	0	0	0	0	0	1	1					
	RET	1	0	0	0	0	0	1	1	1	2	—	—	(SP)←(SP)－1 PC←((SP)) A program counter value is returned from the stack. At this time, a PSW value remains unchanged.
	RETR	1	0	0	1	0	0	1	1	1	2	○	○	(SP)←(SP)－1 (PC)←((SP)) (PSW)4～7←((SP)) A program counter value is returned from the stack. At this time, the PSW bits 4－7 are also returned from the stack. Used for a return from an interrupt.
Flag	CLR C	1	0	0	1	0	1	1	1	1	1	○	—	C←0 Clears the carry flag.

■ Summary of Instruction Sets(Continued)

Gr.	Mnemonic	D7	D6	D5	D4	D3	D2	D1	D0	Byte	Machine Cycle	Flags Affected C	Flags Affected AC	Description
Flag	CPL C	1	0	1	0	0	1	1	1	1	1	○	—	(C)←(C) Inverts the carry flag.
	CLR F0	1	0	0	0	0	1	0	1	1	1	—	—	(F0)←0 Clears the flag F0.
	CPL F0	1	0	0	1	0	1	0	1	1	1	—	—	(F0)←(F0) Invents the flag F0.
	CLR F1	1	0	1	0	0	1	0	1	1	1	—	—	(F1)←0 Clears the flag F1.
	CPL F1	1	0	1	1	0	1	0	1	1	1	—	—	(F1)←(F1) Inverts the flag F1.
Timer/Counter	MOV A, T	0	1	0	0	0	0	1	0	1	1	—	—	(A)←(T) Transfers the timer/counter contents to the accumulator.
	MOV T, A	0	1	1	0	0	0	1	0	1	1	—	—	(T)←(A) Transfers the accumulator contents to the timer/counter.
	STRT T	0	1	0	1	0	1	1	1	1	1	—	—	Starts the timer. The timer/counter is counted up every 3 machine cycles.
	STRT CNT	0	1	0	0	0	1	0	1	1	1	—	—	Starts the counter. The counter is incremented every time the T1 pin is changed from High to Low.
	STOP TCNT	0	1	1	0	0	1	0	1	1	1	—	—	Stops the timer/counter.
	EN TCNTI	0	0	1	0	0	1	0	1	1	1	—	—	Enables a timer/counter interrupt. An interrupt is caused by a timer/counter overflow.
	DIS TCNTI	0	0	1	1	0	1	0	1	1	1	—	—	Clears a timer/counter interrupt request flag to disable an interrupt
Control	EN I	0	0	0	0	0	1	0	1	1	1	—	—	Enables an external interrupt. An interrupt sequence takes place, if a Low−level signal is applied to the INT pin.
	DIS I	0	0	0	1	0	1	0	1	1	1	—	—	Disables an external interrupt.
	SEL RB0	1	1	0	0	0	1	0	1	1	1	—	—	(PSW)4←0 Selects the register bank 0. A working register assumes addresses 0−7.
	SEL RB1	1	1	0	1	0	1	0	1	1	1	—	—	(PSW)4←1 Selects the register bank 1. A working register assumes addresses 18−1F.

■ Summary of Instruction Sets(Continued)

Gr.	Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Byte	Machine Cycle	Flags Affected C	AC	Description
Control	SEL MB0	1	1	1	0	0	1	0	1	1	1	—	—	(DBF)←0 Selects the program memory bank 0. The JMP and CALL instructions jump to 0—7FF.
	SEL MB1	1	1	1	1	0	1	0	1	1	1	—	—	(DBF)←1 Selects the program memory bank 1. The JMP and CALL instructions jump to 800—7FF.
	ENTO CLK	0	1	1	1	0	1	0	1	1	1	—	—	Causes a clock to be outputted from the test pin T0. This is cleared by MCU reset only.
Others	IDL	0	0	0	0	0	0	0	1	1	1	—	—	Places MCU in the HALT mode to halt internal operation.
	NOP	0	0	0	0	0	0	0	0	1	1	—	—	(PC)←(PC)+1 No operation. Causes the program counter to be incremented.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
 Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

20080805